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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,327	02/26/2004	Austin H. Lesea	X-1026-1D US	3981

24309 7590 10/27/2004

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,327	LESEA, AUSTIN H.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *091304*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Response to the Restriction requirement filed September 13, 2004 has been entered. Claims 1 – 4 were elected without traverse and claims 5 – 9 have further been canceled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 – 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In **claim 1**, lines 13 – 18, the limitation '...first and second transistors programmable to provide low and high resistances ...' is considered vague and indefinite since it is not clear to one of ordinary skill in the art what values of the resistances are considered low, or high.

Clarification is required in order to overcome this type of rejection.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 – 4 are rejected under the judicially created doctrine of double patenting over claims 1 – 8 of U. S. Patent No. 6,735,110 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: the memory device having SEU resistant circuitry, comprising:

a first inverter …; a second inverter …; a first transistor …; a second transistor …; wherein each of the first and second transistors has a gate coupled to a gate bias voltage source, which controls the conductive state to provide the output resistances (patented claims 1, 2). The first and second transistors are PMOS transistors (patented claim 3) and have floating bodies (patented claim 1), and the memory device comprises a configuration memory cell of a programmable logic device (patented claim 8).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Golke et al. (US Pat 6,058,041).

Regarding **claims 1**, Golke et al. disclose a memory device having single event upset resistant circuitry, comprising:

a first inverter having a first input node and a first output node (fig. 3, inverter on the left having a first input node and a first output node);

a second inverter having a second input node and a second output node (fig. 3, inverter on the right having a second input node and a second output node);

a first transistor having a first source/drain contact coupled to the first input node and a second source/drain contact coupled to the second output node (fig. 4, top transistor in the middle of the two inverters);

a second transistor having a third source/drain contact coupled to the second input node and a fourth source/drain contact coupled to the first output node (fig. 4, bottom transistor in the middle of the two inverters),

wherein each of the first and second transistors has a gate to which a gate bias voltage is applied to put the first and second transistors into a partially conductive state to provide low and

high resistances (inherent in circuit shown by Golke where access/gate transistors, as in fig. 1, can modulate high or low resistances depending on the applied gate biases—basis characteristics of the transistors. See also col. 2, lines 3 – 28).

Regarding **claim 2**, Golke et al. also disclose the memory device of claim 1, wherein the first transistor and the second transistor having floating bodies (col. 4, lines 9 – 10).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golke et al. in view of Rockett (US Pat 6,369,630 B1).

Regarding **claim 4**, Golke et al. disclose the memory device of claim 1, except wherein the memory device comprises a configuration memory cell of a programmable logic device. However, this feature has been shown by Rockett (col. 8, lines 19 – 37). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature shown by Rockett to the disclosures by Golke et al., so that reconfigurable logic circuits can be changed to form a different logic function on demand (Rockett, col. 1, lines 31 – 57).

Regarding **claim 3**, the first and the second transistors being PMOS are considered design choice since the claim did not specify any uniqueness of such limitation as mandatory.

10. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golke et al. in view of Rockett (US Pat 6,369,630 B1).

Regarding claim 4, although Golke et al. did not disclose the feature in which the first and second transistors provide high and low resistances whose values are to minimize single event upset, or soft errors; however, the concept has been shown by Woodruffet et al., (fig. 1 & abstract, two programmable resistors 140 and 144 are to provide high and low resistances for different memory operations). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Woodruff et al. to the disclosure of Golke et al. so that immunity to soft errors or single event upset increases.

Regarding **claim 3**, the first and the second transistors being PMOS are considered design choice since the claim did not specify any uniqueness of such limitation as mandatory.

Conclusion

11. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
October 19, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800